Influence of Channel Thickness Variation on Temperature and Bias Induced Stress Instability of Amorphous SiInZnO Thin Film Transistors

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Received November 1, 2016; Accepted December 1, 2016

TFTs (thin film transistors) were fabricated using a-SIZO (amorphous silicon-indium-zinc-oxide) channel by RF (radio frequency) magnetron sputtering at room temperature. We report the influence of various channel thickness on the electrical performances of a-SIZO TFTs and their stability, using TS (temperature stress) and NBTS (negative bias temperature stress). Channel thickness was controlled by changing the deposition time. As the channel thickness increased, the threshold voltage ($V_{th}$) of a-SIZO changed to the negative direction, from 1.3 to -2.4 V. This is mainly due to the increase of carrier concentration. During TS and NBTS, the threshold voltage shift ($V_{th}$) increased steadily, with increasing channel thickness. These results can be explained by the total trap density ($N_t$) increase due to the increase of bulk trap density ($N_{bulk}$) in a-SIZO channel layer.

Keywords: Amorphous SiInZnO, Instability, Negative bias temperature stress, Activation energy

1. INTRODUCTION

TAOS (transparent amorphous oxide semiconductors) based TFTs (thin film transistors) are promising candidates as the next generation materials for backplane devices of active matrix displays, to replace conventional amorphous silicon (a-Si) due to their superior electrical properties, such as high mobility of $>10$ cm$^2$/V s, good uniformity, and good subthreshold swing. In addition, TAOS TFTs are transparent in visible light because of their large band gap ($>3.3$ eV). Moreover, TAOS materials are suitable for flexible displays, such as rollable and foldable, providing low cost process like roll to roll. Mobility is an important electrical parameter in TAOS; however, it greatly depends on the channel materials, gate insulators, applied voltage, and TFT structures. The leading TAOS materials are indium-zinc-oxide (a-IZO) based materials, due to their excellent electrical properties, foremost among them being amorphous indium-gallium-zinc-oxide (a-IGZO) [1-3]. However, since gallium is very expensive and rare, gallium-free materials like ZTO (zinc-tin-oxide) [4], HIZO (hafnium-indium-zinc-oxide) [5], SZTO (silicon-zinc-tin-oxide) [6], and a-SIZO (amorphous silicon-indium-zinc-oxide) are rapidly studied. Recently, Lee et al. reported that a-SIZO TFT has high field effect mobility and low temperature process below 150$^\circ$C [7]. This material can contribute to flexible display due to low manufacturing temperature. Moreover, high manufacturing temperatures over 250$^\circ$C, such as post-annealing and passivation process, are critical options to use flexible substrates. However, the electrical stability of TAOS TFTs for flexible electronic devices is a serious problem under BS (bias stress), TS (temperature stress), and IS (illumination stress). Electrical stability is still studied in terms of manufacturing temperature, doping the carrier generation suppressor materials, such as Zr, Hf, Si and Al, the contact between gate insulator and channel interface, and the control of channel thickness. The channel thickness is an important parameter in TFT.

In this paper, a-SIZO TFTs with different channel thickness, using RF (radio frequency) magnetron sputtering at below 150$^\circ$C, have been fabricated. The stability of a-SIZO TFTs was measured by TS and NBTS. The influence of the channel thickness on the electrical performances of a-SIZO TFTs were also investigated by analyzing activation energy falling late.
2. EXPERIMENTS

The a-SIZO channels were deposited by RF magnetron sputtering on substrate (SiO$_2$ (200 nm)/p-type Si). The target of a-SIZO used was 1 wt. % Si-incorporated SIZO (In$_2$O$_3$/ZnO ratio = 3:1), magnetron sputtering power density of 30 W, process pressure of 4 mTorr, and Ar flow ratio of 30 sccm at room temperature. The various thicknesses for a-SIZO films were controlled by changing the deposition time. All films were annealed at 150°C for 2 hrs in a thermal furnace with air ambience. Channel and source/drain electrodes were patterned by the conventional photolithography and wet-etching processes. The Ti (10 nm)/Al (50 nm) source/drain electrodes were fabricated using ebeam and thermal evaporator, respectively, followed by lift-off process. The patterned channel width and length were 250 μm and 50 μm, respectively.

Figure 1 shows a schematic diagram of the a-SZTO TFT. The electrical performance and the electrical stability were measured in the dark, using a semiconductor parameter analyzer (EL 423, ELECS Co.) and vacuum probe station (HP4145B, Hewlett-Packard Co.). The a-SIZO channel thickness was measured to be about 12, 24, and 36 nm by -step (Alpha-step D-100, KLA Tencor Co.).

3. RESULTS AND DISCUSSION

Figure 2(a) shows the drain current ($I_D$)-gate voltage ($V_G$) characteristics of a-SIZO TFTs with drain voltage ($V_D$) of 5.1 V and gate voltage from -20 V to 40 V. Their electrical performance, such as field effect mobility ($\mu_{FE}$), threshold voltage ($V_{TH}$), on-off current ratio ($I_{ON/OFF}$), and subthreshold slope (S.S), are summarized in Table 1. The electrical performance of a-SIZO TFTs shifted to negative due to the increase of carrier concentration. The $\mu_{FE}$ was calculated by equation (1) [8]:

$$\mu_{FE} = \frac{L}{W} \frac{g_m}{C_{ox}}$$  

where $g_m$ is the trans-conductance, $C_{ox}$ is the oxide capacitance of the gate insulator, and W and L are channel width and length, respectively.

Also, it is observed that the S.S value increased significantly. This can be attributed to the change of the total trap density ($N_T$).

Figure 2(b) shows the total trap density of a-SIZO TFTs with various channel thickness. We calculated of $N_T$ value from the S.S by using equation (2) [9]:

$$N_T = N_{IT} + N_{Bulk} = \frac{S S \log(e)}{KT/q} \cdot \frac{1}{1 - \frac{1}{N_c}}$$  

where $N_{IT}$ is the interfacial trap density, $N_{Bulk}$ is the bulk trap density, T is the absolute temperature, k is the Boltzmann constant, q is the electronic charge, and Ci is the capacitance of the gate insulator. According to equation (2), as channel thickness increased, the $N_T$ values rapidly rise from 5.2×10$^{10}$ to 1.0×10$^{12}$ cm$^{-2}$. a-SIZO TFTs have same gate insulator/channel interface since the channel thickness is controlled only by deposition time, and hence the $N_T$ values are dependent on the $N_{Bulk}$ values. In general, the S.S value was affected by NIT, which in turn was affected by channel thickness in thin films.

Figure 3 and Figure 4 shows the evolution of transfer curves of a-SIZO TFTs with various channel thickness under temperature stress and their activation energy ($E_a$), from 298 to 333 K. The $V_{TH}$ is clearly observed to be negatively shifted. The $\Delta V_{TH}$ of a-SIZO TFTs under temperature stress is related with the increase in thermally excited electrons. As the temperature increased, the captured electrons are emitted from trap sites by thermal energy. The values of $\Delta V_{TH}$ of a-SIZO TFTs were measured at 1.21, 1.35, and 2.29 V, as channel thickness increased at intervals of 12 nm, from 12, 24 to 36 nm, respectively. As mentioned, 12 nm of channel thickness has less trap sites, and therefore few electrons were emitted from the trap site. We estimated the $E_a$ depends on the change of gate voltages in the forbidden band gap by fitting the temperature stress for different channel thicknesses. The $E_a$ was investigated by using equation (3) [10]:

$$I_D = I_{DO} \cdot \exp \left(- \frac{E_a}{KT} \right)$$  

where $I_{DO}$ is the prefactor, k is Boltzmann constant, T is the absolute temperature.